

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claim 1 is amended to address the objection noted in paragraph 3 of the Office Action.

Claims 1-12, 14-18, and 20 are pending in this application. Claims 1-12 and 14-18 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 5,714,775 to Inoue et al. (herein “Inoue”). Claim 20 was rejected under 35 U.S.C. § 103(a) as unpatentable over Inoue.

Addressing the above-noted rejections, those rejections are traversed by the present response.

Initially, applicants note the claims are amended by the present response to clarify features recited therein. Specifically, independent claim 1 now further recites “a source diffused layer between first gate electrodes of the first gate electrode group”. The other independent claims are amended to recite similar features.

The claimed features are believed to be clearly supported by the original specification, see for example Figures 7 and 9 in the present specification showing the N-type source diffused layer 14 formed between trench gates 18a in the substrate.

The claims recite a semiconductor device including a first gate electrode group having a plurality of gate electrodes formed on a semiconductor substrate to be away from each other at first equal spacings, a first gate insulating film formed on both of sidewall-surfaces opposed to each other of a first gate electrode of the first gate electrode group, a channel region formed along the gate insulating film on both of the sidewall-surfaces opposed to each other of the first gate electrode of the first gate electrode group, a source diffused layer between first gate electrodes of the first gate electrode group, a source contact having a portion formed separated from the first gate electrode of the first gate electrode group by a

second spacing greater than the first spacing, and source regions for electrically interconnecting the first gate electrode and the source contact.

In the semiconductor device of the claimed invention, the source diffused layer is formed between gate electrodes, and a source contact is not formed adjacent to or on a plurality of the source diffused layers, see Figure 7 in the present specification as a non-limiting example. With such a structure a plurality of source diffused layers can be collected to a source region, and the source region can be connected with a source contact. As a result electrical charges flowing from the source diffused layers are passed through the source region to reach the source contact. Since one source contact includes a plurality of trench gates, with the claimed invention the number of source contact areas can be reduced. Since a number of channel regions can be formed in a given region with a minimum design spacing, a channel density can also be increased, and the device resistance of a MOSFET can be set low with such a configuration.

The basis for the outstanding rejection references Figure 14 of Inoue to disclose a source contact portion 42 and source regions 38.

The claims now recite both “a source diffused layer” and “source regions”. Inoue does not disclose or suggest both such layers as claimed.

More particularly, in Inoue the regions 38, which are emitter regions in Inoue, would correspond to the now claimed “source diffused layer”. In that respect Inoue does not disclose an element corresponding to the claimed “source regions”. Alternatively, Inoue does not disclose the newly claimed “source diffused layer”.

Moreover, Inoue fails to disclose source diffused layers collected to a source region, which is connected with the source contact, and the source contact not formed adjacent to or on the source diffused layers. In the structure shown in Figure 14 of Inoue the source contacts 44, which are emitter electrodes, are directly formed on the source emitter regions

38. Since one source contact connects with one source region 38, which indicates one source contact corresponds to one source region 38, the number of source contact areas cannot be reduced. Thus, Inoue cannot realize benefits as can be realized by the claimed invention.

In view of these presently submitted claim amendments and foregoing comments, applicants respectfully submit Inoue does not disclose all the features recited in the claims as currently written. Thereby, the claims as currently written are believed to distinguish over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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